Tito Khan MSc BSc (Hon) CEng MIEE

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Career Experience

Software Engineer **Stein Systems, London 08/2000 -**

- Start up company involved in DSP algorithm development – gained experience in a wide range of work from networking computers, setting up multiple boot machines, design tools, etc.
- Particular interest in analyis of digital transmission systems using probabilistic mathematical models to assess effect of degradations such as intersymbol interference, bandlimiting, white noise on bit error rate.
- Algorithmic searches through user groups for novel DSP techniques.
- Experience with web design tools – Macromedia Dreamweaver and Fireworks.
- Evaluator7T development board ARM Developer Suite (Code Warrior, AXD) on evaluation board for Samsung KS32C50100 microcontroller with an ARM7 core
- Visual C++ / OOD
- Suse Linux 8.1

Consultant Software Engineer **ERICCSON EUROLAB, Nürnberg Germany 07/2000 -04/2002**

- DSP engineer 3rd Generation BTS (UMTS Node B)
- TI C6203 DSP, layer 2 /3 data on the user plane and also control plane.
- Data on the control plane was used to compute parameters and set up and maintain a database for various requested channels. This data together with user data packets was used to subsequently produce “service packets”. Assembled packets contained information required to configure the next processing unit (FPGA channel coder) in the chain.
- Low level working with PCCPCH, SCCPCH/PICH, FACH, DCH (setup and reconfiguration) channels.
- OSE DSP RTOS platform.
- Implementation of loopback functions incorporating ASIC and DSP.
- Reproduction of complex failure scenarios found during integration tests conducted in Sweden, debugging and subsequent code testing.
- Extensive use of test tools, including JTAG emulator, logic analyser, RTOS provided tools (e.g. core dump analyser) etc. An Ethernet based diagnostic tool designed in-house across several sites in Europe, provided a consistent debug interface across four other processors on the board was used to set up these scenarios. Additionally, developed test tools in C to facilitate these processes.
- Also involved in re-design activities using UML real time extension Rational Rose Real Time. This was an OOP using C++ as the implementation language.

Experience: Software design, structured and OOP, debugging, maintenance, Clearcase, ClearDDTS
Courses Attended: Rational Rose Real Time

Senior DSP Engineer **LUCENT TECHNOLOGIES, Swindon, Wiltshire, England, 03/99 – 06/2000**

- DSP firmware engineer 3rd Generation BTS (UMTS Node B)
- Involved in the early stages of the project where benchmarking, DSP and RTOS selection, hardware software partitioning, and other important design decisions were made. This led to the architectural design and subsequent work breakdown.

- The DSP team responsible for this baseband processing task comprised of around 13 engineers, approximately half of whom were located in the US. More specifically, worked in the receiver design team and on the architectural design of the diagnostic system. This work involved working with people across a wide range of departments from system simulation, system integration, and RF performance to hardware integration.

Experience: Architectural design of baseband processor on BTS, architectural design of diagnostic subsystem, software design.
Languages: C
Courses: UMTS Air Interface, OSE RTOS, and SPW.

Senior DSP Engineer **LUCENT TECHNOLOGIES, Swindon, Wiltshire, England, 07/99 – 03/99**

Involved in the STRU2™ (Subscriber Transceiver Unit) project which is a DS CDMA system, part of the Airloop™ (fixed wireless access) system. In the project, fulfilled the following roles:

- **Boot Code Design:**
- Flexible boot up mechanism allowing download in a number of ways.
- On-core fixed point DSP (CWDSP1640 Oak Core) and implemented in gates in the ASIC designed in house. The code was written with a combination of C and assembler.
- **CDMA/QPSK Demodulation Code:**
- Automatic Gain Control, transmit power control, scrambling and other essential functions required in a CDMA system.
- Also **Delay Lock Loop Filter** design – to optimise the code lock procedure using MATLAB (analysis of early late filters as error detector, s- curve,etc. (Proportional / Integral loop filter design)
- Algorithm Implementation in Q15 and Q31and integration into working system
- **Code Integration:**
- Changing multi-disciplined teams at various phases in the projects. E.g.ASIC and hardware engineers during hardware integration, RF engineers during radio integration and engineers from various parts of the system during system integration.
- **System Integration:**
- Close working in laboratory with other departments, required use of spectrum analyser and other RF tools as well as logic analysers and call generators, etc.
- During this phase some of the more obscure system level bugs were discovered.
- **Maintenance**
- Maintenance of Analogue Devices ADSP2181 DSP code on previous STRU release , which was the processor on STRU1.
- **DSP Support:**
- Support to the other sections such as the RF and ASIC departments to facilitate testing and verification of their parts of the system.
- Manufacturing support in development of low level routines designed to run on a PC. The software was used to configure a PC card designed in house, which was in turn used to control the STRU2 during manufacturing tests.

Experience: Algorithm development, simulation and software design, system integration, system test.
Languages: C, Oak assembly, Analogue Devices ADSP2181 assembly.
Courses: VHDL, vxWorks (RTOS), C++ and Object Oriented Design.

DSP Design Engineer **ADTRANZ, Plymouth, England 04/93 - 06/99**

As a DSP engineer, worked on the following real time embedded projects:

- **Alternative Modulation Schemes:**
- Investigation into various digital modulation schemes (FSK, PSK) to determine the most appropriate one for our requirements of a low rate data channel along rail tracks.
- Investigation into coherent detectors (matched detectors and correlation), analysis of error probability in presence of white noise.
- Produced report which provided an analysis of the schemes, and recommendations (modulation scheme, data rates, frequency specifications, etc.)
- **Demonstration of DSP based Demodulator**
- Following analysis, demonstrated the scheme designing and implementing a non coherent Binary FSK system
- Demodulation filters designed using the Motorola DSP56001 and associated development tools.

- Algorithms developed using Matlab, used in conjunction with DFDP to generate coefficients for the elliptical IIR and FIR (Hilbert, averaging) filters.
- Pole–Zero analysis used to determine stability pre and post quantisation.
- **Track Circuit Meter:**
- Demodulation algorithms incorporated into this tool using structured coding standards (Yourdon based) on the fixed point ADSP2103 DSP.
- Dual processor required to make accurate measurements of data signals in the presence of interfering signals.
- Low level design of peripheral drivers including (UART configuration for diagnostics, timer channel, ADC etc).
- Deign and implementation of autoranging functions, true RMS, frequency selective and DC voltage and current measurements as well as being able to demodulate FSK signals on the track.
- MATLAB used for algorithm development and testing.
- Code designed and documented in accordance with the structured design methodology used within the company (TICKIT approved, based on Yourdon).
- Design of hardware/software interface to allow a PC to issue commands and receive data in order to test the test the DSP software in isolation from the master processor..

Vehicle Receiver Modification:

- The vehicle receiver is an ADSP 2101 based, rack mounted unit designed to receive and demodulate FSK signals travelling in the rails. It also provides some diagnostic facilities via a RS232 serial link. Responsible for the maintenance of the software and the repair of faulty units.

Modelling of Cable/Rail Arrangement:

- Involved in the modelling of the inductance of rail and cable arrangements using an integral method and also Neumann's method.
- Mathematical models were developed using MathCAD and simulations performed using Pspice in an Orcad environment.
- Interface with university consultancy group

Experience: DSP algorithm development, filter design, structured software development, microprocessor based design, digital design, Algorithmic State Machine design methodology, analogue design, and mathematical analysis.
Languages: C, DSP56001 assembly, ADSP2101 assembly, and 8051 assembly/C.
Software: Windows, Word for Windows, Quick C, Orcad, Pspice, Matlab, MathCAD, CADSTAR, PVCS, Timeline, RelCalc.
Courses: DSP in Communications, EMC and the Technical Construction File, Advanced Digital Communications, Certificate in Management.

Development Engineer, GEC ALSTHOM SIGNALLING, Borehamwood, Herts, England 12/89 – 08/91
The work was varied and had gained experience in a broad range of disciplines. First project was in the development of a microprocessor based system used in the automatic testing of signalling equipment for rail systems. Other projects included the design of test equipment to interface to existing rigs. In final project, worked as part of a team responsible for the development of a track side decoder.
Experience: Hardware design (analogue design, microprocessor based development), C programming.
Languages: C, BASIC, PASCAL, and 6809 ASSEMBLY.
Software: Windows, WordStar, Word for Windows, Turbo C, dBase IV, and Orcad.
Courses: Presentation skills, C programming

Education Details

MSc in Telecommunications and Information Systems, University of Essex 1992
Main subjects: signals & systems, transmission systems, probability, real time systems, switching systems, digital transmission, neural networks, radio frequency engineering and image processing.
MSc project: The use of S-parameters in EMC modelling. Involved extensive research into newly published papers to apply a recent technique for quantifying radiation from a three port device in a microstrip line. Programs were written in C to produce results graphically
BSc Hons Electronic Eng. Class: Upper Second.
University of Manchester Institute of Science and Technology 1989

Final year options: communication engineering, information theory and coding, control engineering and management studies.
Final year project: Design of a four-bit digital to analogue converter using CMOS technology. Involved investigation of analogue design techniques, simulation/test of designed circuit (HSPICE-II) and mathematical analysis
Certificate in Management (Part time) University of Plymouth 1994
Main subjects studied: Marketing, people and organisations, accountancy, employment law, personal and interpersonal skills, and economics, computing for business and operations management.
4 'A' Levels (Maths, Further Maths, Physics, Chemistry) 10 'O' levels 1984 Mill Hill School, London.

Referees

Available on request.